REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1-12 have been examined and are all the claims pending in the application.

Formal Matters

Applicant thanks the Examiner for reviewing and initialing the documents in the Information Disclosure Statement submitted March 7, 2007.

Claim Rejections -- 35 U.S.C. § 103(a)

Claims 1–12 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,710,938 to Dahl *et al.* (hereinafter "Dahl") in view of U.S. Patent No. 6,308,279 to Toll *et al.* (hereinafter "Toll").[1] Applicant respectfully traverses the rejection.

For example, claim 1 recites an array-type processor with the feature of a plurality of state control units which change a configuration of a multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by contexts composed of instruction codes.

In rejecting claim 1, the Examiner cites to Fig. 1, item 20 of Dahl as allegedly teaching an array-type processor with a state control unit which changes a configuration of a multiplicity of processor elements and causes successive transitions of operating states of the multiplicity of processor elements for each operating cycle by means of contexts that are composed instruction codes.

[1] Item 5 states that the rejection is a rejection under 35 U.S.C. § 102(a). However, Applicant notes that the section heading and corresponding discussion indicate a 103(a) rejection. Accordingly, Applicant believes this item 5 contains a typographical error.

Dahl discusses a manually operated (col. 2, lines 57–61; col. 4, lines 7–11) single control module located in a *separate microprocessor* (col. 2, lines 57–61; col. 3, lines 61–62) for a static configuration (col. 4, lines 11–16; col. 9, lines 18–21) of individual and independent sections of a data processing array (col. 4, lines 19–22; col. 2, lines 51–54) *of processors* (col. 3, lines 45–48) running individual programs *without context switching* (col. 4, lines 35–37; col. 9, lines 37–39) until the system is rebooted (col. 9, lines 11–16).

Applicant respectfully submits that Dahl does not disclose or teach a plurality of state control units that change the configuration and cause successive transitions of operating states of processor elements for *each operating cycle by contexts*, *within an array-type processor*. Dahl discloses an operator-set single configuration for loading different programs into pre-assigned individual processors. Toll does not remedy the deficiency, as Toll is directed to a power mode transition signal for multi-threaded processors.

With further regard to claim 1, claim 1 recites the feature of state control units temporarily halting operations of processing element areas that correspond to a prescribed number of operating states that are set to a context during an operating cycle during which the operating states do not occur. In rejecting the claims, the Examiner alleges a processing element without a task to perform will inherently halt processing so as to save power. The Applicant respectfully disagrees and submits Toll discusses external chipsets (col. 1, lines 48–51; col. 3, lines 1–3 and lines 35–37) to control the power state of processors thereby showing power control of processing is not an inherent quality of processors. Further, the Examiner states (page 3) a processor must be told to stop processing by passing it an instruction, which additionally shows power control of processors is not an inherent quality of processors.

Further still, the Examiner cites to Toll (col. 2, lines 19–34 and 52–55) as teaching halting individual processors or individual threads of a multiprocessor system. Applicant respectfully points to the following sentence of Toll (col. 2, lines 56–58) in that the sections of Toll cited by the Examiner describe the problem to be solved and a lack of workable solution ("may cause a problem" at 36–37, "would slow the process down" at 41–42, "no guarantee" at 42, and "is difficult" at 46). The external control chipset and signals described by Toll do not teach or describe an array-type processor with state-control-units (as components of the array-type processor) which halt individual processing elements of the processor, as recited by claim 1.

Accordingly, Applicant respectfully submits that claim 1 is patentable over Dahl, either alone or in combination with Toll for at least the aforementioned reasons. Reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 103(a) are respectfully requested.

Claims 2 and 3 recite features similar to claim 1, and accordingly Applicant respectfully submits that claims 2 and 3 are also patentable over Dahl either standing alone or in combination with Toll, for at least the same reasons. The remaining rejected claims are patentable based on of their respective dependencies.

Examiner's Response to Arguments

The Examiner quotes 37 C.F.R. § 1.111(c) on page 7 of the Office Action. However, Applicant respectfully submits that the Amendment filed April 6, 2007 complies with the cited section.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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